

MS-7120

Version 1B

INTEL (R) Brookdale-GV Chipset

Willamette/Northwood/533Prescott 478pin mPGA-B Processor Schematics

CPU: Willamette/Northwood/533Prescott
mPGA-478B Processor

System Chipset:

INTEL Brookdale-GV GMCH + ICH4

On Board Chipset:

BIOS -- FWH

LPC Super I/O -- W83627HF-AW

Clock Generator -- CY28349

AC'97 Codec -- RealTek ALC650/655

Onboard Lan Chipset-- RealTek RTL8101L

Expansion Slots:

AGP2.0 SLOT * 1 (PCI-BUS)

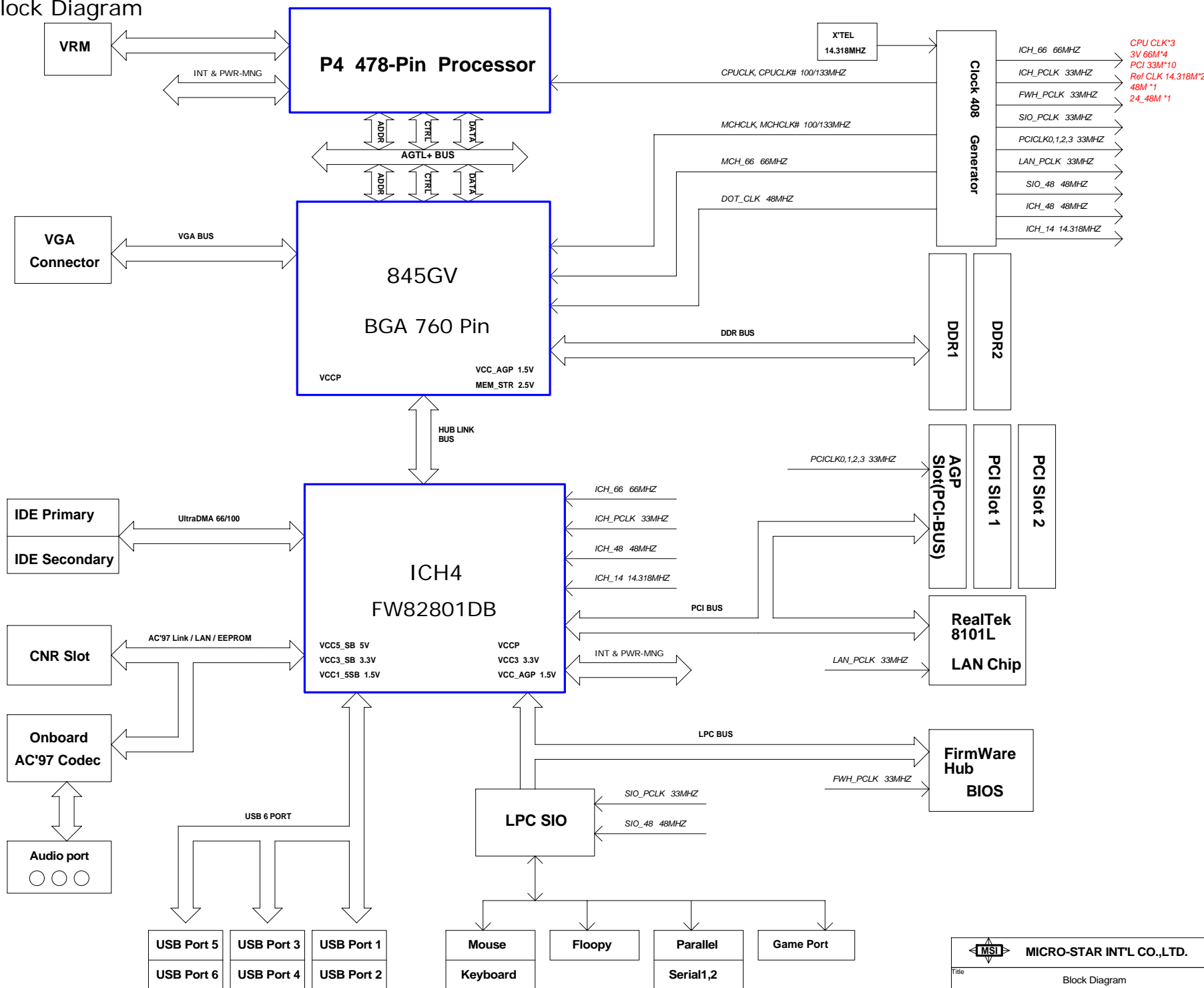
PCI2.2 SLOT * 2

Platform: Micro ATX

MODEL/Ver	ORCAD Config.	Function Description	Option	ERP Number
MS7120-0A	cfg7120GV-LAN	GV+LAN	L	601-7120-A10
MS7120-100	cfg7120GV-LAN	GV+LAN	L	601-7120-010
MS7120-100	cfg7120GV-A	GV+LAN+Buzzer	A	601-7120-02S
MS7120-1A	cfg7120GV-LAN	GV+LAN+USB-ESD	L	601-7120-03S
MS7120-1A	cfg7120GV-LAN	GV+LAN+USB-ESD+MS7	L	601-7120-07S

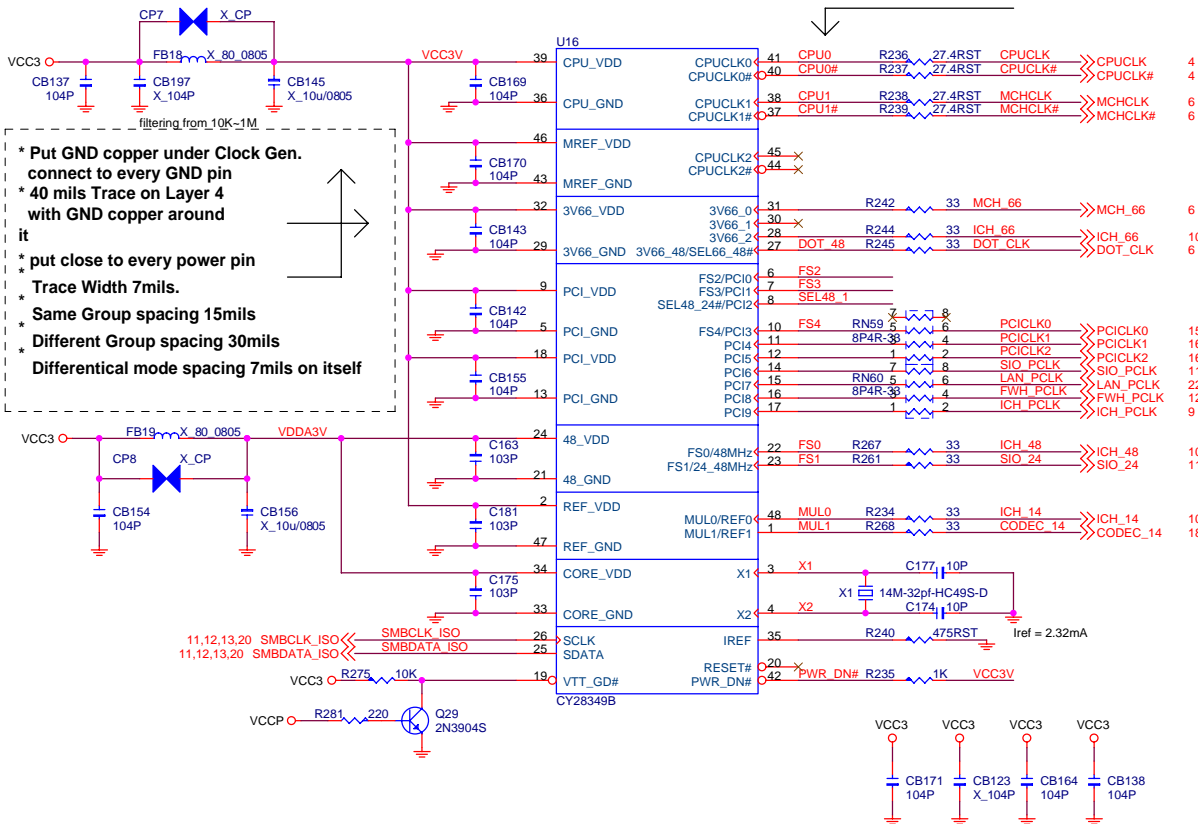
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Block Diagram



CLOCK GENERATOR BLOCK

*Trace < 0.5"



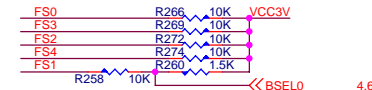
Shut Source Termination Resistors



Trace less 0.2"

49.9ohm for 50ohm M/B impedance

CLOCK STRAPPING RESISTORS



FS4	FS3	FS2	FS1	FS0	FSB (MHz)
1	1	1	0	1	100 MHz
1	1	1	1	1	133 MHz

SEL48 1 R270 X 10K VCC3V

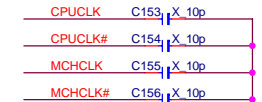
DOT 48 R241 10K

0 Set Pin 27 48MHz

MUL0 R233 X 10K VCC3V

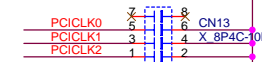
MUL1 R262 10K VCC3V

Pull-Down Capacitors



ICH 66 C158 X 10p

MCH 66 C157 X 10p



SIO_PCLK 2 C162 X 10p

LAN_PCLK 4 C163 X 10p

FWH_PCLK 6 C164 X 10p

ICH_PCLK 8 C165 X 10p

ICH 14 C152 10P

SIO 24 C178 X 10P

ICH 48 C180 X 10P

CODEC 14 C182 X 10P

DOT_CLK C160 X 10P

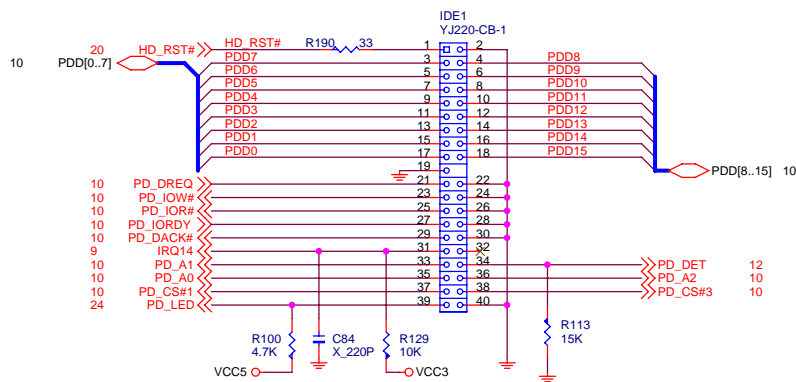
Ioh=6*Iref

Voh=0.71V

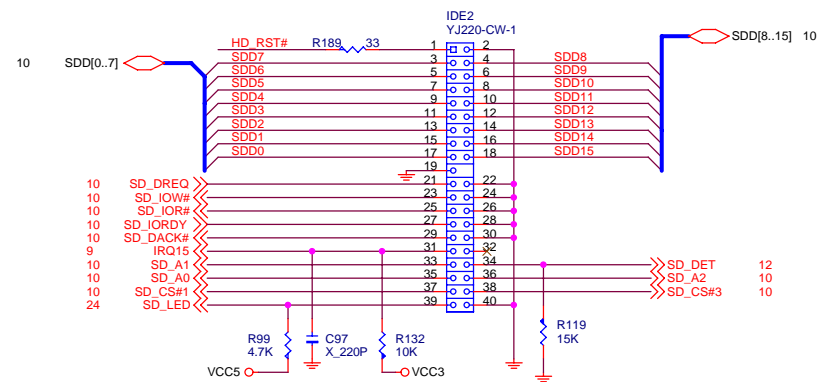
used only for EMI issue

Trace less 0.2"

PRIMARY IDE BLOCK



SECONDARY IDE BLOCK

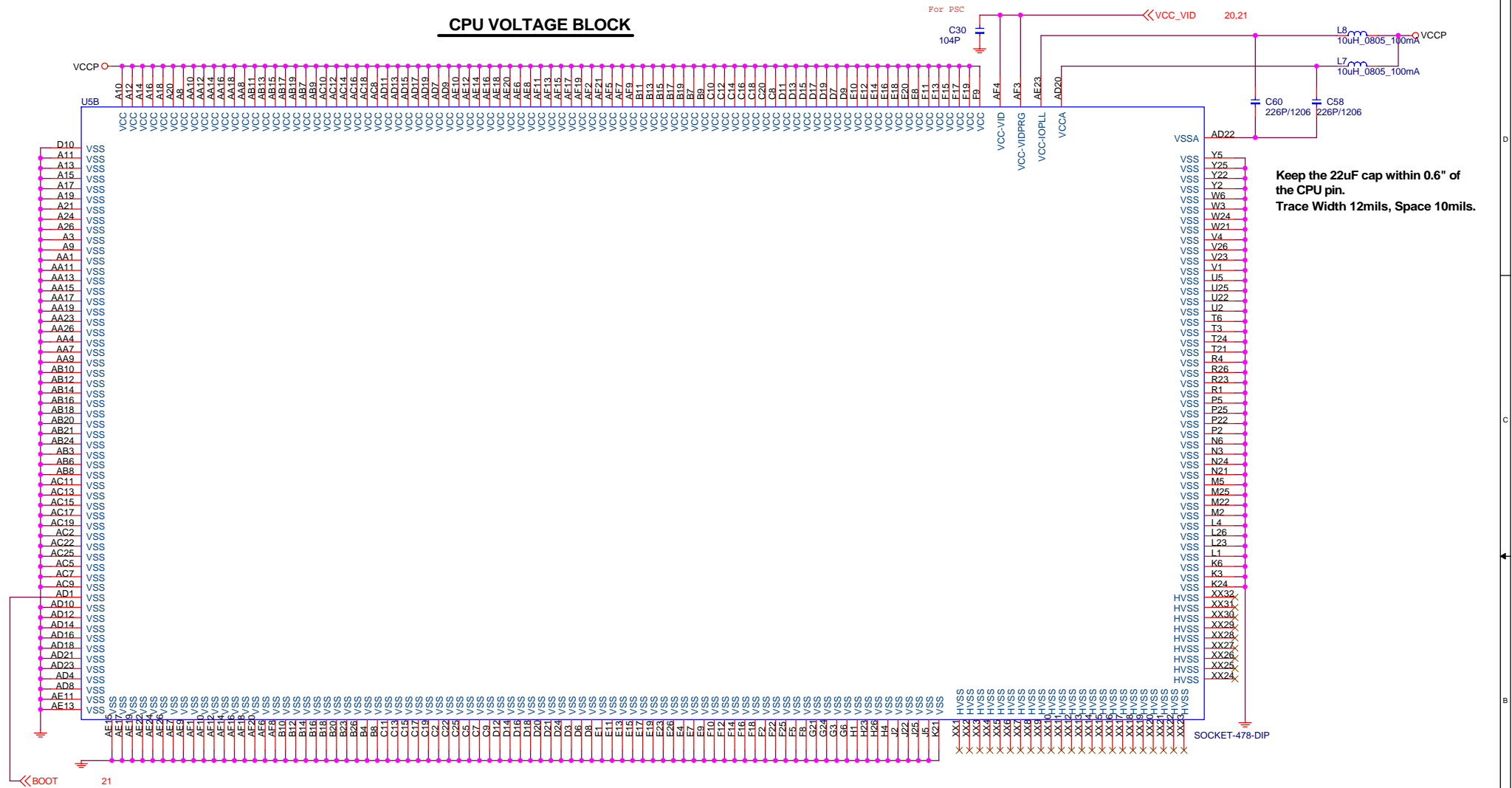


ATA100 IDE CONNECTORS

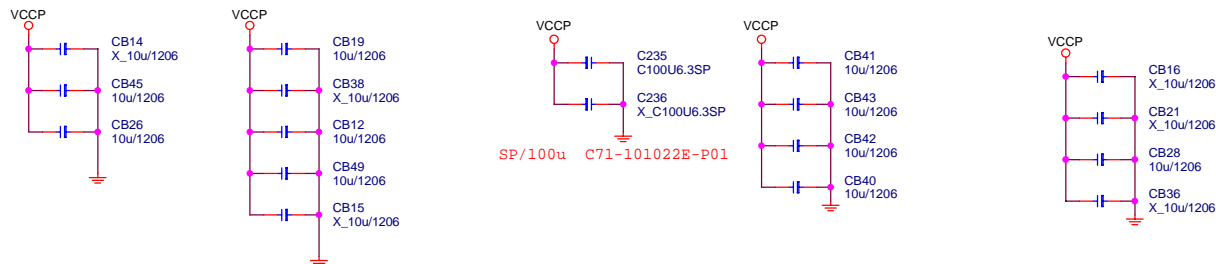
- * Trace Width : 5mils
- * Trace Spacing : 7mils
- * Length(longest)-Length(shortest)<0.5"
- * Trace Length less than 5"

MICRO-STAR			
Title: CLOCK GEN & ATA100 IDE			
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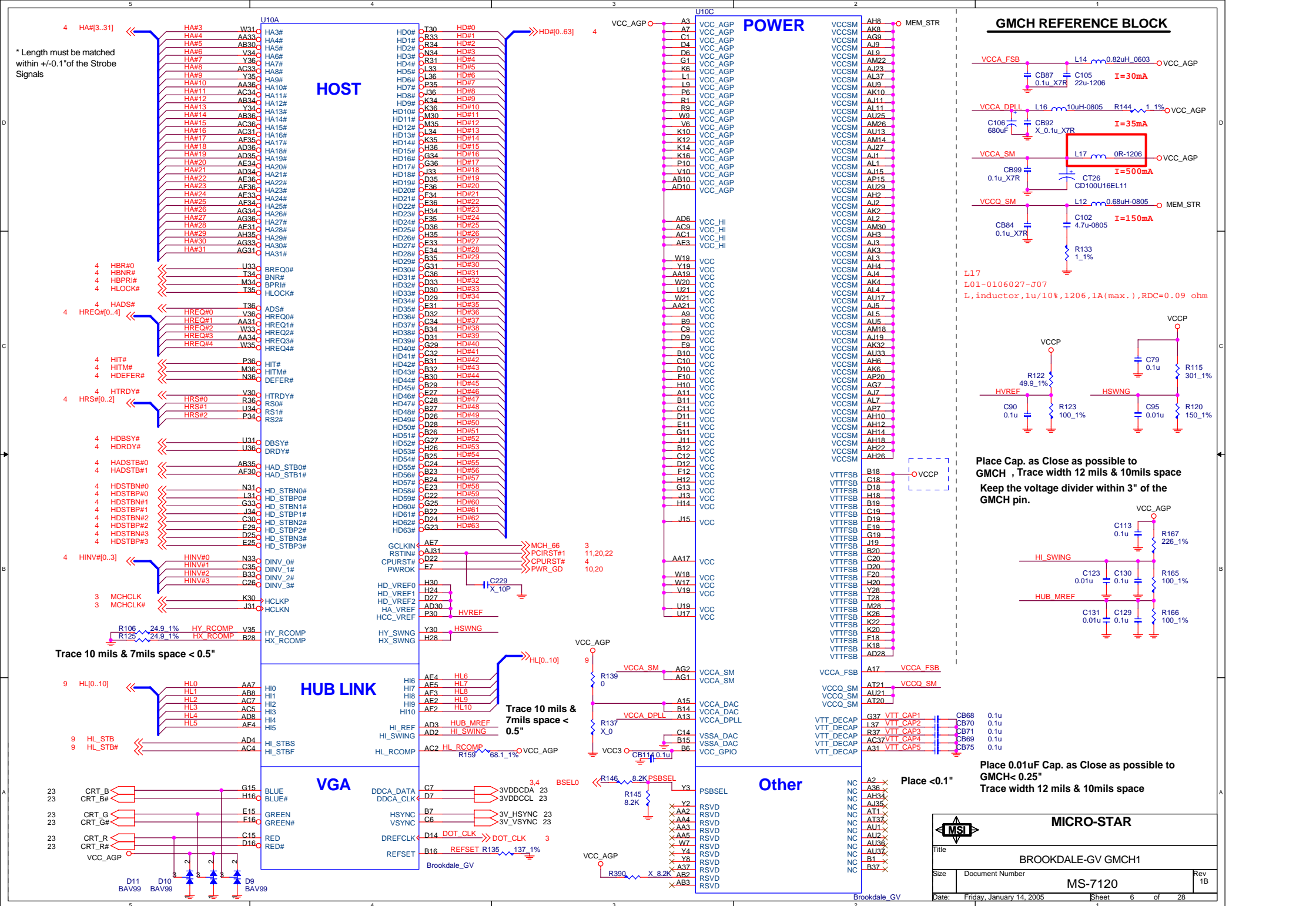
CPU VOLTAGE BLOCK



CPU DECOUPLING CAPACITORS



MICRO-STAR			
Title	INTEL mPGA478-B CPU2		
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13,14 DDRMD[0..63]

U10B
DDRMD0 AN4 SDQ0
DDRMD1 AP2 SDQ1
DDRMD2 AT3 SDQ2
DDRMD3 AP5 SDQ3
DDRMD4 AN2 SDQ4
DDRMD5 AP3 SDQ5
DDRMD6 AR4 SDQ6
DDRMD7 AT4 SDQ7
DDRMD8 AT5 SDQ8
DDRMD9 AR6 SDQ9
DDRMD10 AT9 SDQ10
DDRMD11 AR10 SDQ11
DDRMD12 AT6 SDQ12
DDRMD13 AP6 SDQ13
DDRMD14 AT8 SDQ14
DDRMD15 AP8 SDQ15
DDRMD16 AP10 SDQ16
DDRMD17 AT11 SDQ17
DDRMD18 AT13 SDQ18
DDRMD19 AT14 SDQ19
DDRMD20 AT10 SDQ20
DDRMD21 AR12 SDQ21
DDRMD22 AR14 SDQ22
DDRMD23 AP14 SDQ23
DDRMD24 AT15 SDQ24
DDRMD25 AP16 SDQ25
DDRMD26 AT18 SDQ26
DDRMD27 AT19 SDQ27
DDRMD28 AR16 SDQ28
DDRMD29 AT16 SDQ29
DDRMD30 AP18 SDQ30
DDRMD31 AR20 SDQ31
DDRMD32 AR22 SDQ32
DDRMD33 AP22 SDQ33
DDRMD34 AP24 SDQ34
DDRMD35 AT26 SDQ35
DDRMD36 AT22 SDQ36
DDRMD37 AT23 SDQ37
DDRMD38 AT25 SDQ38
DDRMD39 AR26 SDQ39
DDRMD40 AP26 SDQ40
DDRMD41 AT28 SDQ41
DDRMD42 AR30 SDQ42
DDRMD43 AP30 SDQ43
DDRMD44 AT27 SDQ44
DDRMD45 AR28 SDQ45
DDRMD46 AT30 SDQ46
DDRMD47 AT31 SDQ47
DDRMD48 AR32 SDQ48
DDRMD49 AT32 SDQ49
DDRMD50 AR36 SDQ50
DDRMD51 AP35 SDQ51
DDRMD52 AP32 SDQ52
DDRMD53 AT33 SDQ53
DDRMD54 AP34 SDQ54
DDRMD55 AT35 SDQ55
DDRMD56 AN36 SDQ56
DDRMD57 AM36 SDQ57
DDRMD58 AK36 SDQ58
DDRMD59 AP36 SDQ59
DDRMD60 AP36 SDQ60
DDRMD61 AM35 SDQ61
DDRMD62 AK35 SDQ62
DDRMD63 AK34 SDQ63

DDR

DDRMAA0 AN25
DDRMAA1 AN25
DDRMAA2 AP23
DDRMAA3 AK20
DDRMAA4 AL19
DDRMAA5 AL17
DDRMAA6 AP19
DDRMAA7 AP17
DDRMAA8 AN17
DDRMAA9 AK16
DDRMAA10 AK26
DDRMAA11 AL15
DDRMAA12 AN15
DDRMAAB1 AP25
DDRMAAB2 AN23
DDRMAAB4 AN19
DDRMAAB5 AK18
SDQS0 AR2
SDQS1 AT7
SDQS2 AT12
SDQS3 AT17
SDQS4 AR24
SDQS5 AT29
SDQS6 AT34
SDQS7 AL36
SDM0 AP4
SDM1 AR8
SDM2 AP12
SDM3 AR18
SDM4 AT24
SDM5 AP28
SDM6 AR34
SDM7 AL34
MSCKE0 AP13
MSCKE1 AN13
MSCKE2 AK14
MSCKE3 AL13
MSCS0# AL29
MSCS1# AP31
MSCS2# AK30
MSCS3# AN31
DCLK0 AL21
DCLK0# AK22
DCLK1 AN11
DCLK1# AP11
DCLK2 AM34
DCLK2# AL33
DCLK3 AN21
DCLK3# AP9
DCLK4 AN9
DCLK4# AP33
DCLK5 AN34
MSBS0 AN27
MSBS1 AP27
MRAS# AK28
MCAS# AN29
MWE# AP29
SMX_RCOMP AF10
SMY_RCOMP AJ34
M4
N7
N5
N2
P2
P4
D5
B5
C3
C2
D3
D2
E4
F3
F2
F4
E5
C4
B4
B3
V8
U7
M8
L7
H8
G7
G5
W2
L2

DDRMAA[0..12] 13,14
DDRMAAB1 13,14
DDRMAAB2 13,14
DDRMAAB4 13,14
DDRMAAB5 13,14
SDQS[0..7] 13,14
SDM0 13,14
SDM1 13,14
SDM2 13,14
SDM3 13,14
SDM4 13,14
SDM5 13,14
SDM6 13,14
SDM7 13,14
MSCKE[0..3] 13,14
MSCS0# 13,14
MSCS1# 13,14
MSCS2# 13,14
MSCS3# 13,14
DCLK0 13
DCLK0# 13
DCLK1 13
DCLK1# 13
DCLK2 13
DCLK2# 13
DCLK3 13
DCLK3# 13
DCLK4 13
DCLK4# 13
DCLK5 13
MSBS0 13,14
MSBS1 13,14
MRAS# 13,14
MCAS# 13,14
MWE# 13,14
SMX_RCOMP 13,14
SMY_RCOMP 13,14

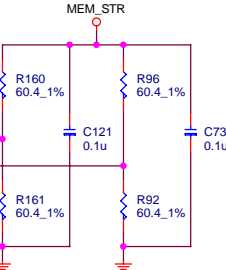
Trace length must as short as possible for SRCVEN

Trace width 12 mil with 12 mil space for SM_VREF.

R387 X_0 Solder
SRC_O# AK24
SRC_I# AL23
C125 0.1u
DDR_VREF
SM_VREF
G_AD0
G_AD1
G_AD2
G_AD3
G_AD4
G_AD5
G_AD6
G_AD7
G_AD8
G_AD9
G_AD10
G_AD11
G_AD12
G_AD13
G_AD14
G_AD15
G_AD16
G_AD17
G_AD18
G_AD19
G_AD20
G_AD21
G_AD22
G_AD23
G_AD24
G_AD25
G_AD26
G_AD27
G_AD28
G_AD29
G_AD30
G_AD31
G_C/BE0#
G_C/BE1#
G_C/BE2#
G_C/BE3#

AGP

G_FRAME#
G_JRDY#
G_TRDY#
G_DEVSEL#
G_STOP#
G_PAR#
G_REQ#
G_GNT#
SBA0
SBA1
SBA2
SBA3
SBA4
SBA5
SBA6
SBA7
SB_STB
SB_STB#
ST0
ST1
ST2
AD_STB0
AD_STB0#
AD_STB1
AD_STB1#
PIPE#
RBF#
WBF#
AGP_VREF
AGP_RCOMP
M4
N7
N5
N2
P2
P4
D5
B5
C3
C2
D3
D2
E4
F3
F2
F4
E5
C4
B4
B3
V8
U7
M8
L7
H8
G7
G5
W2
L2



Trace width 12 mil with 10 mil space. Place 0.1uF <1" to GMCH

MICRO-STAR

Brookdale_GV

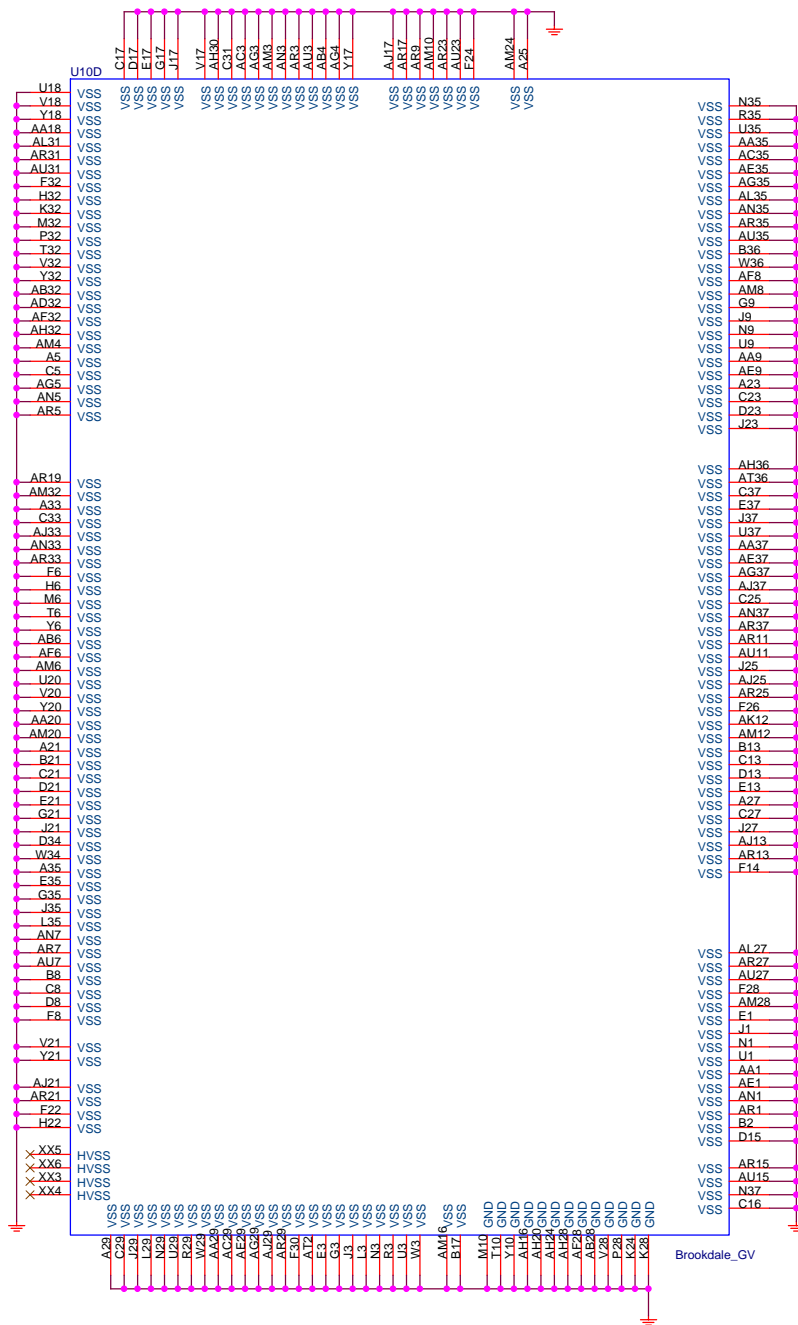
MSI

Brookdale-GV GMCH2

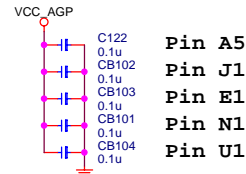
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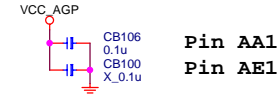
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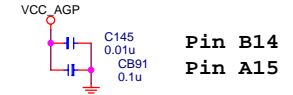
GMCH DECOUPLING CAPACITOR



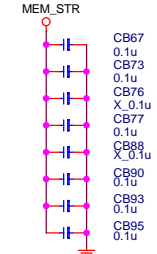
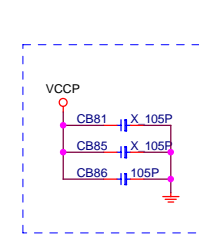
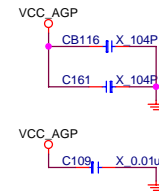
Place decoupling cap
close to GMCH AGP
Interface < 0.1"



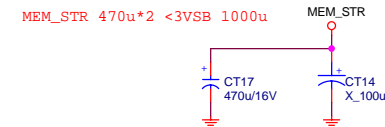
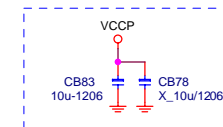
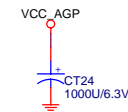
Place decoupling cap
close to GMCH
Hub-Link Interface<
0.1"



Place decoupling cap
close to GMCH DAC
Interface< 0.1"

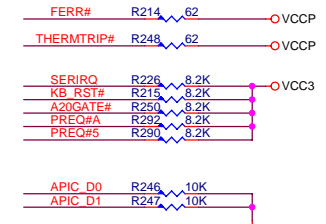
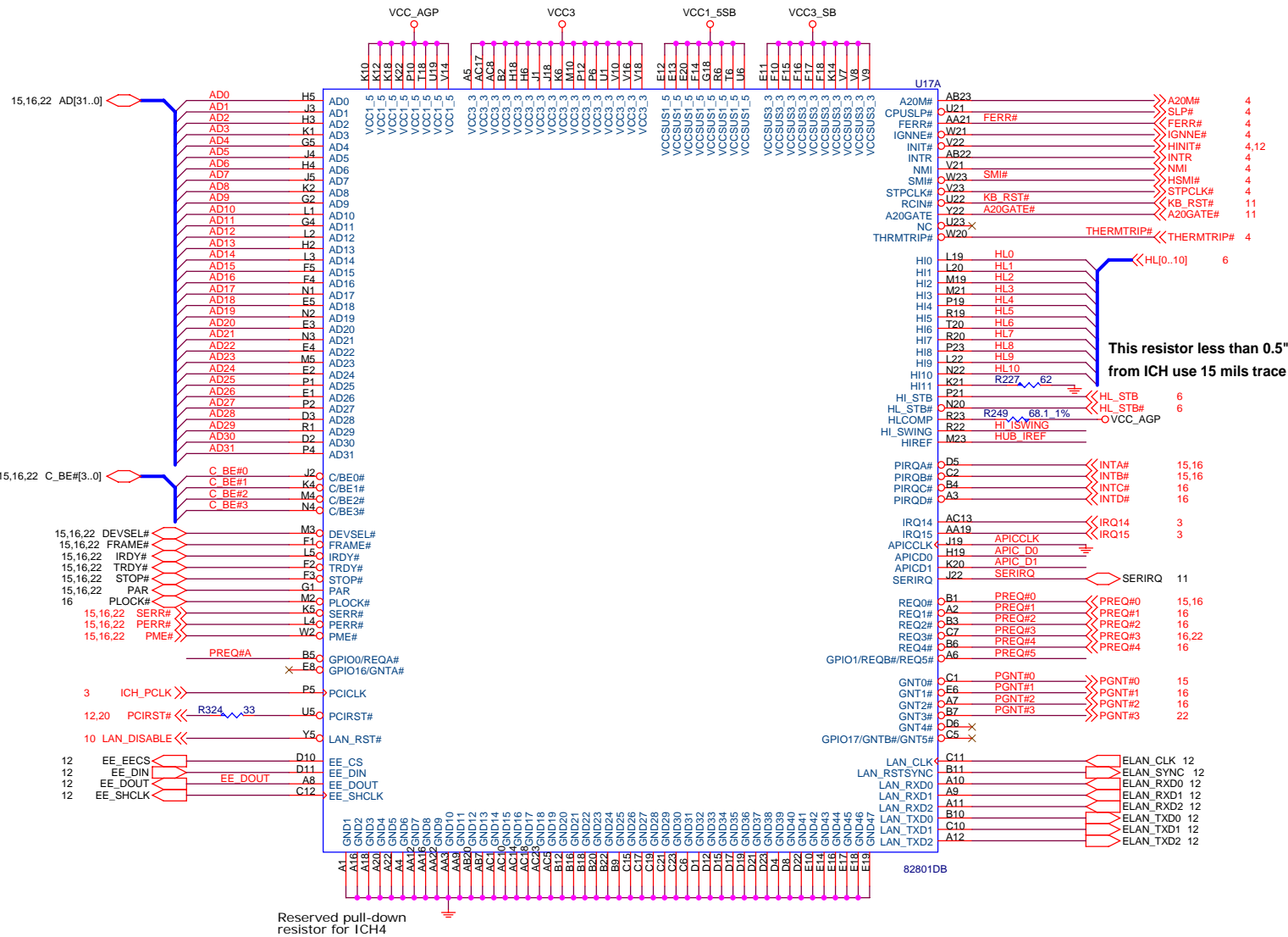


Place decoupling cap
close to GMCH Memory
Interface < 0.1", with
18 mil trace width

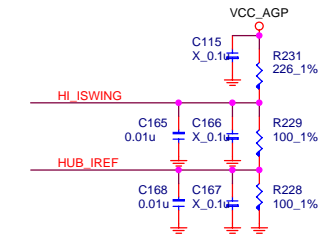


ICH4 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS

ICH4 PULL-UP/DOWN RESISTORS

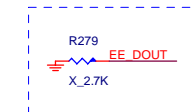


ICH4 REFERENCE VOLTAGE



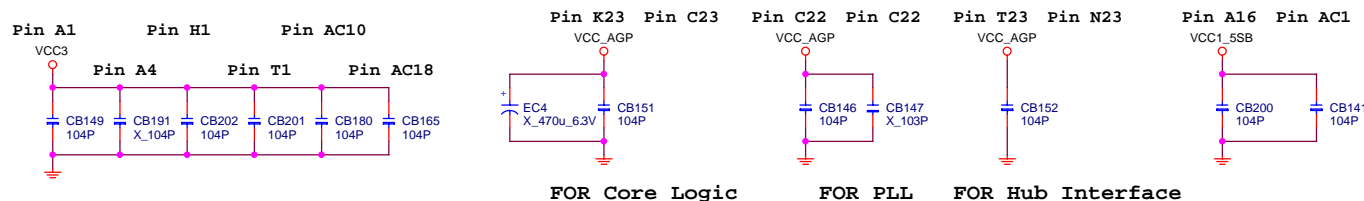
Place Cap. as Close as possible to ICH4 < 0.25"

Trace width use 12 mils and 10mils space

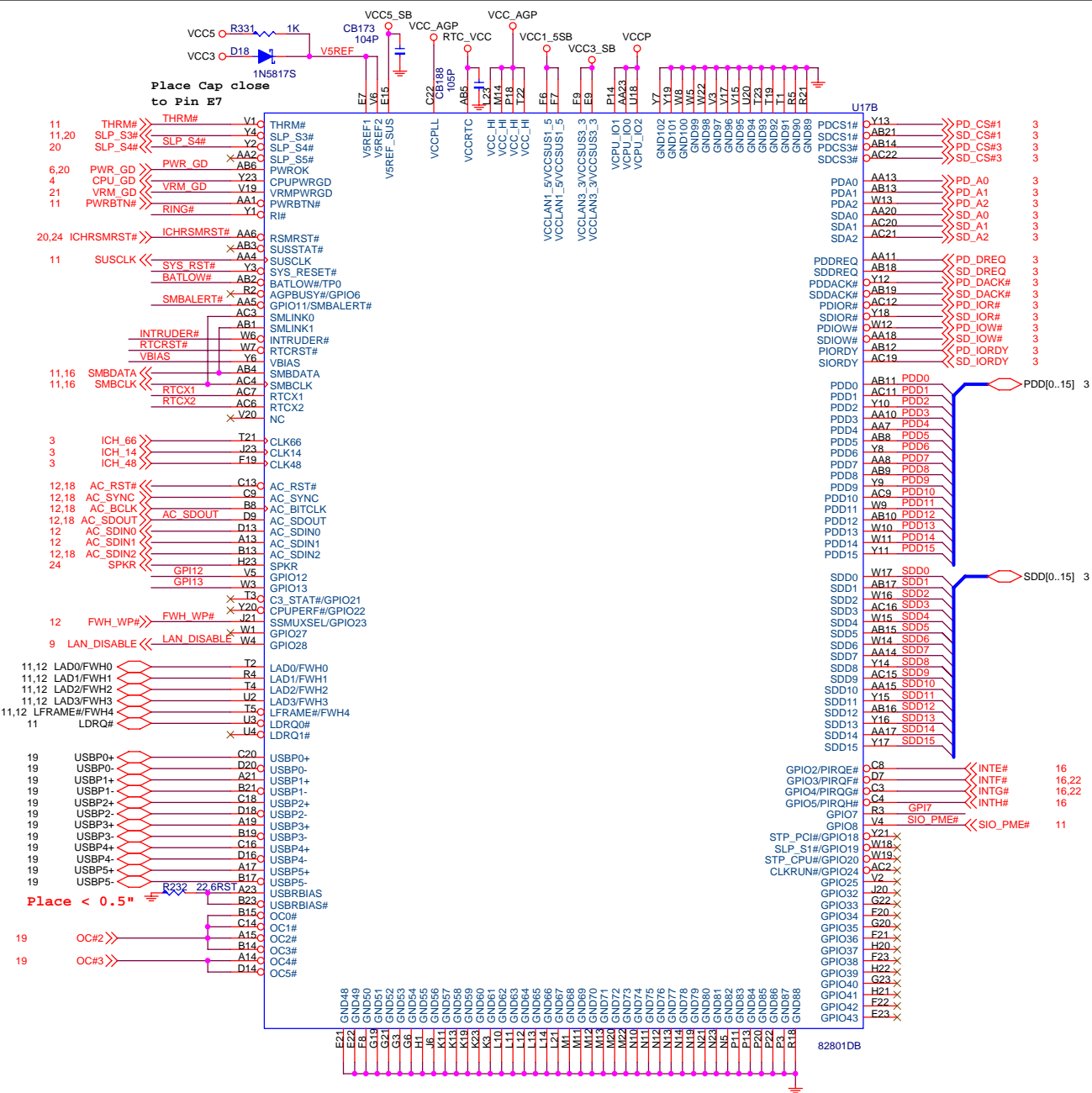


ICH4 DECOUPLING CAPACITORS

Place one 0.1u close to ICH4 <100 mil

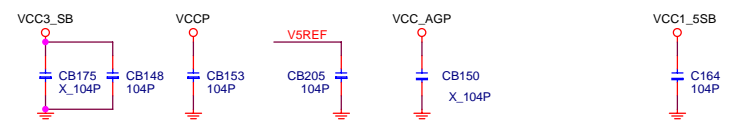


Title ICH4 PCI/HI/LAN			
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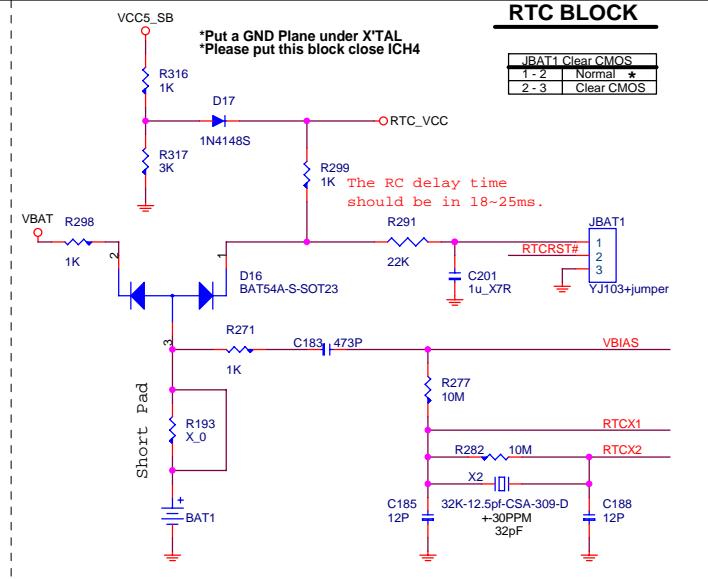
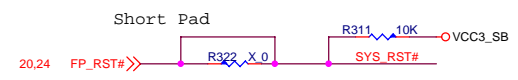


ICH4 DECOUPLING CAPACITOR

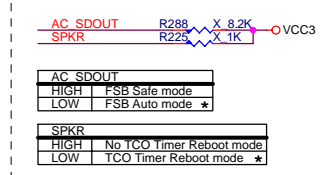
Place one 0.1u close to ICH4 <100 mil



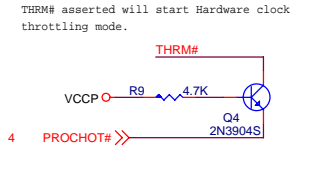
SYSTEM RESET



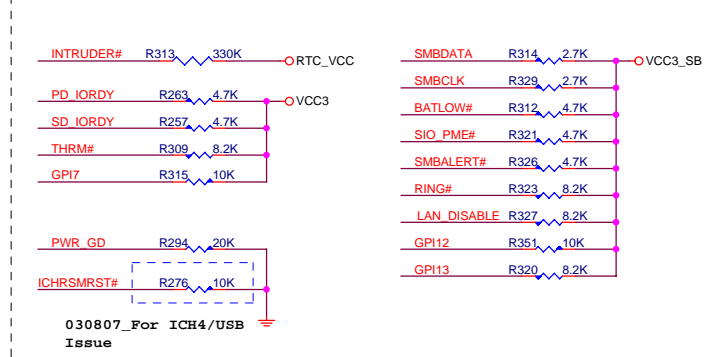
ICH4 STRAPPING RESISTORS



PROCHOT BLOCK

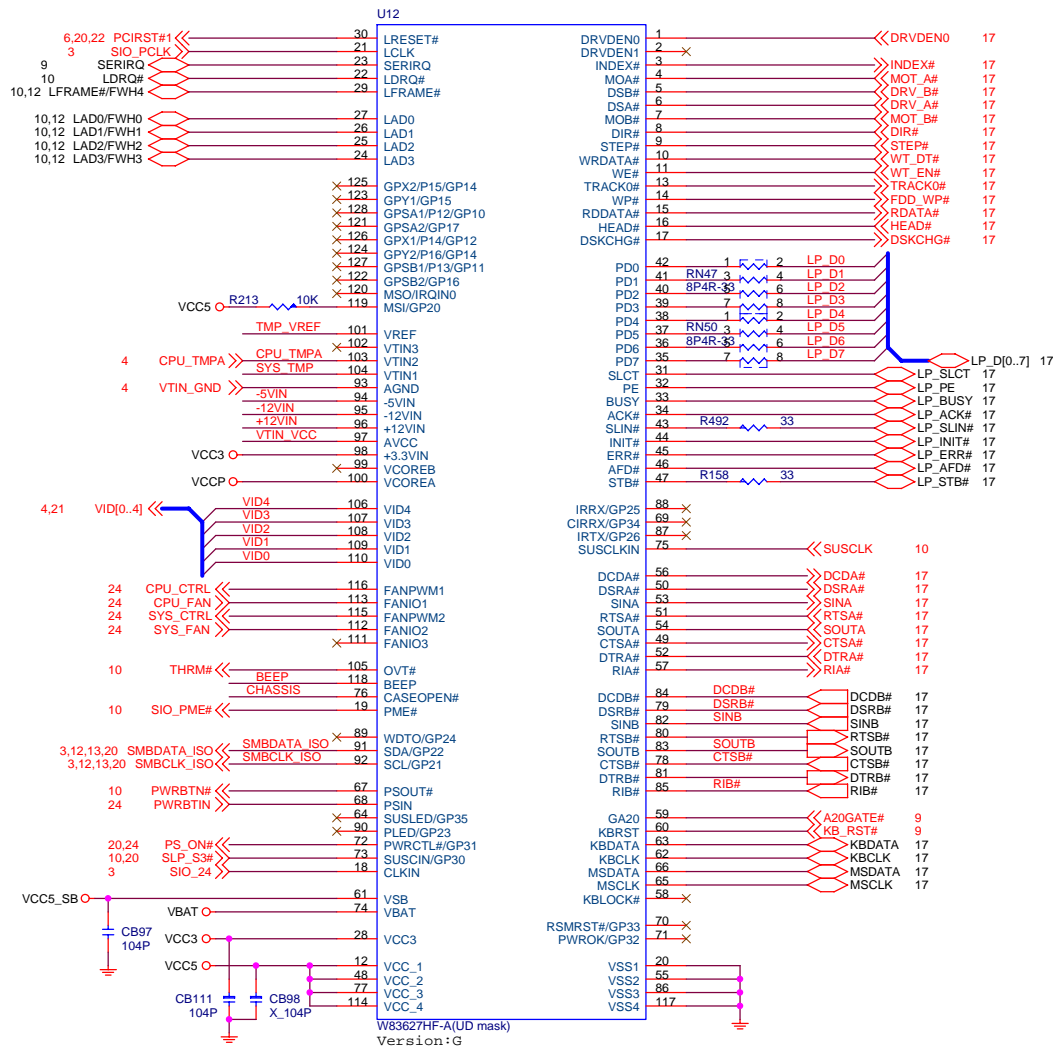


ICH4 PULL-UP/DOWN RESISTORS

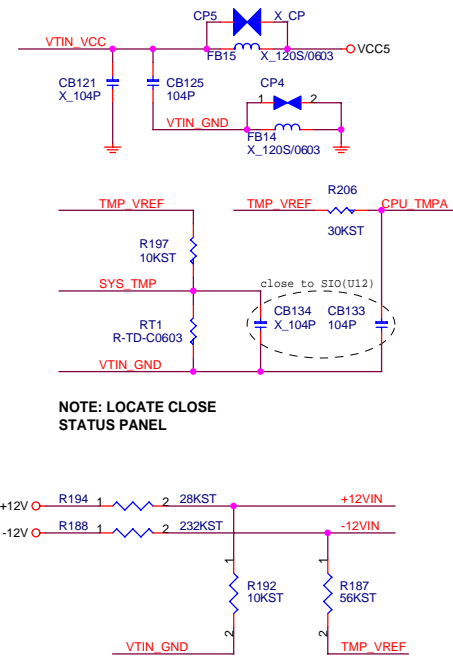


MICRO-STAR logo and title block. Title: ICH4 OTHER. Document Number: MS-7120. Date: Friday, January 14, 2005. Sheet: 10 of 28. Rev: 1B.

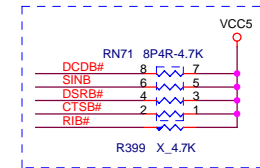
LPC SUPER I/O W83627HF



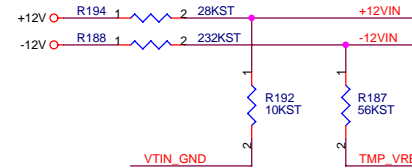
THERMAL RESISTOR BLOCK



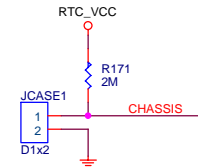
W83627F/HF Ap.15
Avoid Noise From
ULTRAB



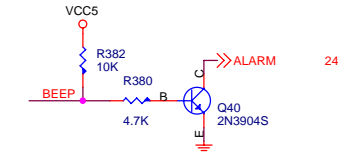
NOTE: LOCATE CLOSE
STATUS PANEL



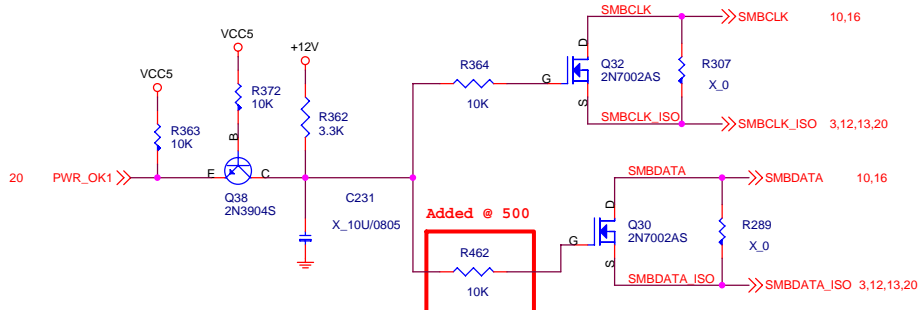
Chassis Intrusion Header



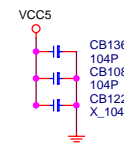
SPEAKER BLOCK



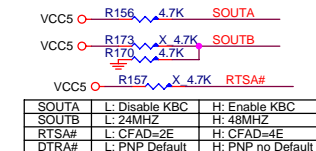
SMBus Isolation



LPC I/O DECOUPLING CAPACITORS

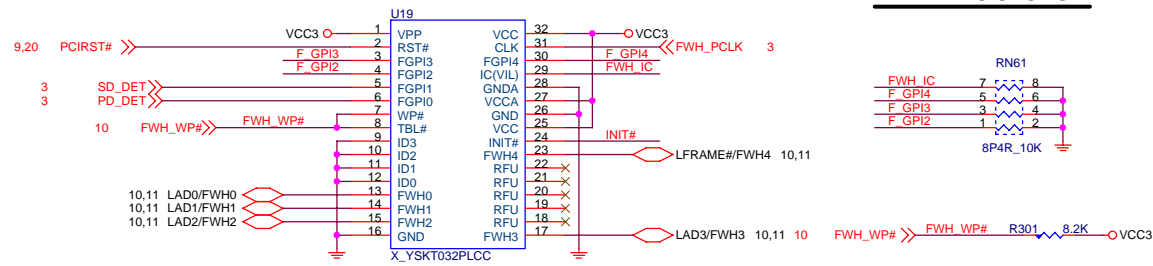


SUPER I/O STRAPPING RESISTOR

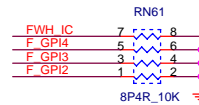


		MICRO-STAR	
Title			
LPC SUPER I/O			
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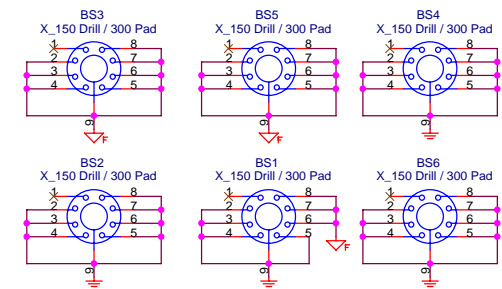
Firmware Hub (FWH)



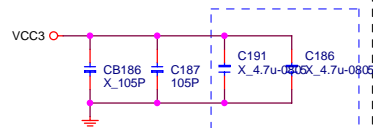
FWH RESISTORS



PCB Mounting Holes



FWH DECOUPLING CAPACITORS

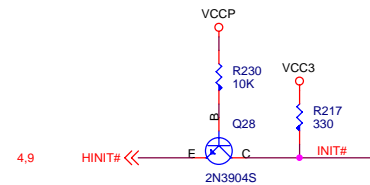


Place Cap. as Close to
FWH < 350 mil

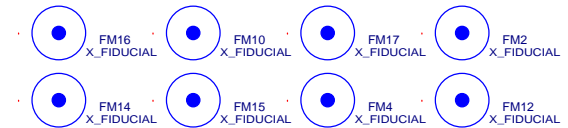
FWH write protect

BIOS_WP BIOS Update	
SHORT	Flash Write Disable
OPEN	Flash Write Enable (Default)

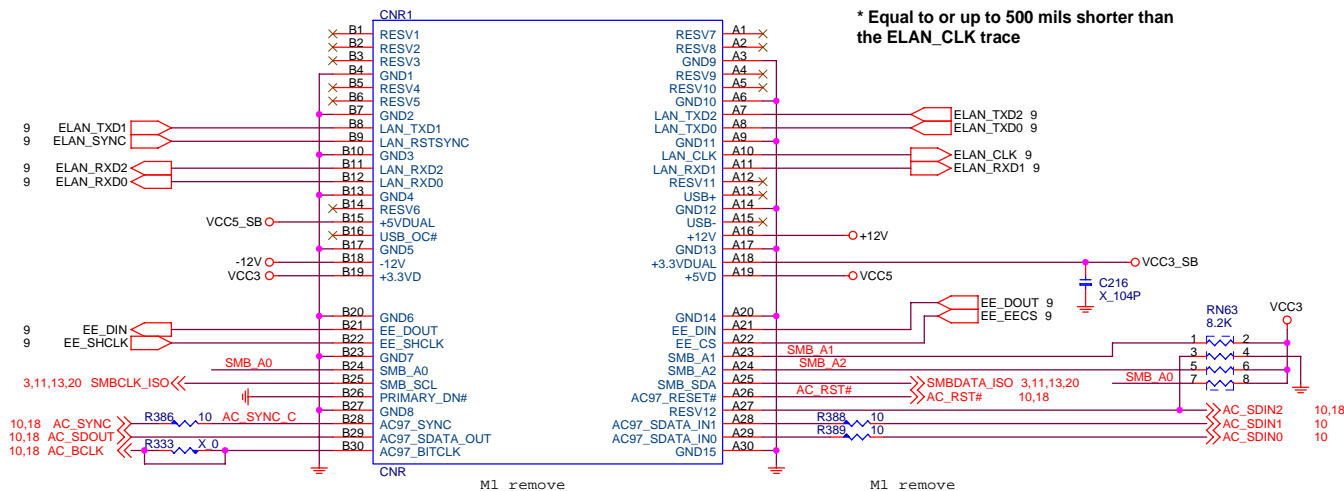
FWH INIT Signal Voltage Translation Block



PCB Fiducials



CNR RISER

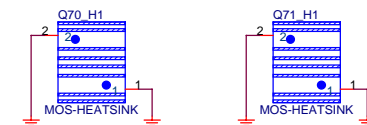


- * LAN Trace width : 5 mils
- * AC'97 Trace Spacing : 10 mils
- * Maxium trace length < 9.5"
- * Equal to or up to 500 mils shorter than the ELAN_CLK trace

SIMULATION TRACE



MOSFET HEATSINK



MICRO-STAR

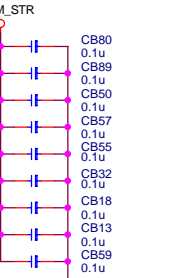
Title	FWH & CNR & Manual Part
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Size	Document Number
	MS-7120

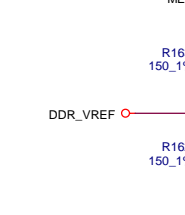
Date: Friday, January 14, 2005 Sheet 12 of 28

SYSTEM MEMORY

7,14 DDRMD[0..63] <<



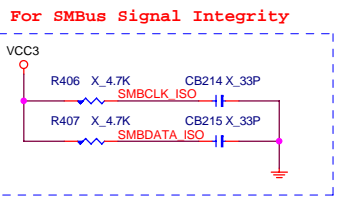
7,14 MWE# << MWE#



Keep the voltage divider within 1" of DIMM1.
Trace width 12 mil with 12 mil space.
Place 104p Cap. near the DIMM

DDR DIMM SOCKET

DDR1
Close to North-Bridge

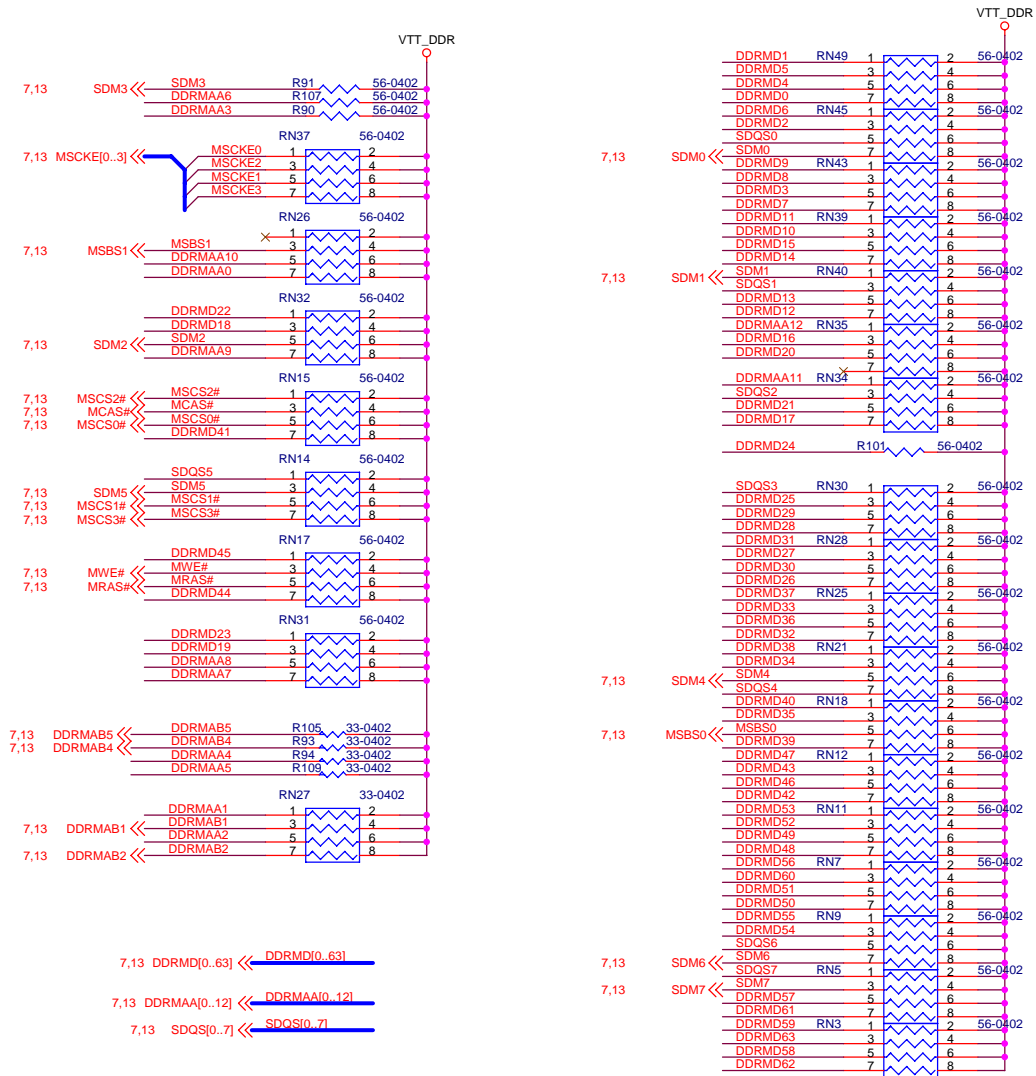


DDR DIMM SOCKET

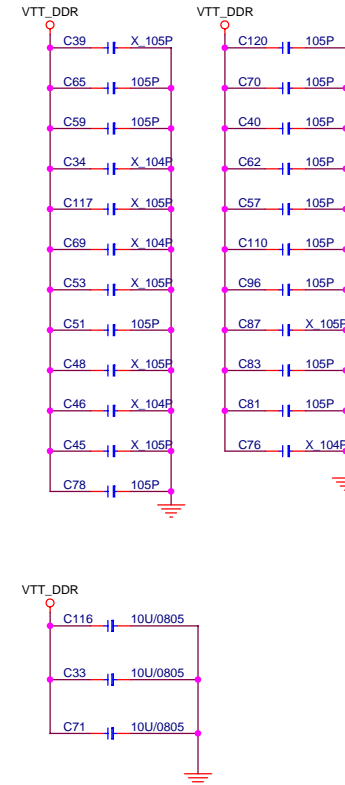
DDR2

MSI		
Title		
DDR DIMM1 & 2		
Size		Rev 1B
Document Number		MS-7120
Date: Friday, January 14, 2005		Sheet 13 of 28

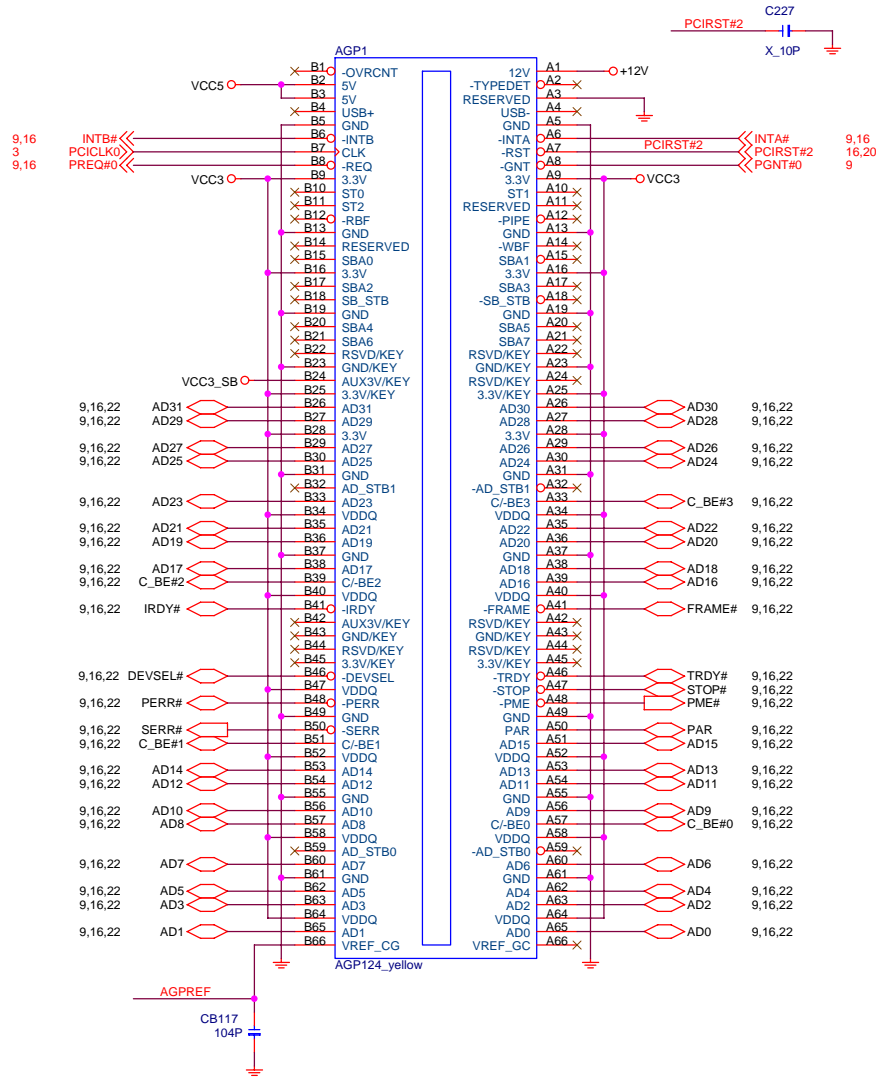
DDR TERMINATORS



TERMINATION DECOUPLING

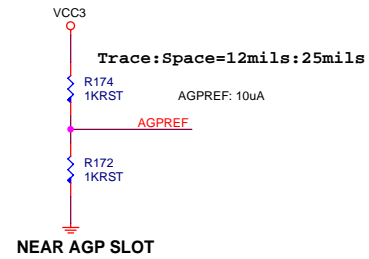


AGP UNIVERSAL 2X/4X SLOT



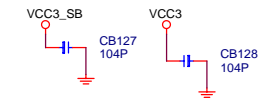
MASTER = PREQ0
INTA#

AGP SIGNAL REFERENCE CIRCUIT



NEAR AGP SLOT

AGP SLOT DECOUPLING CAPACITORS



MICRO-STAR

Title

AGP SLOT

Size

Document Number

MS-7120

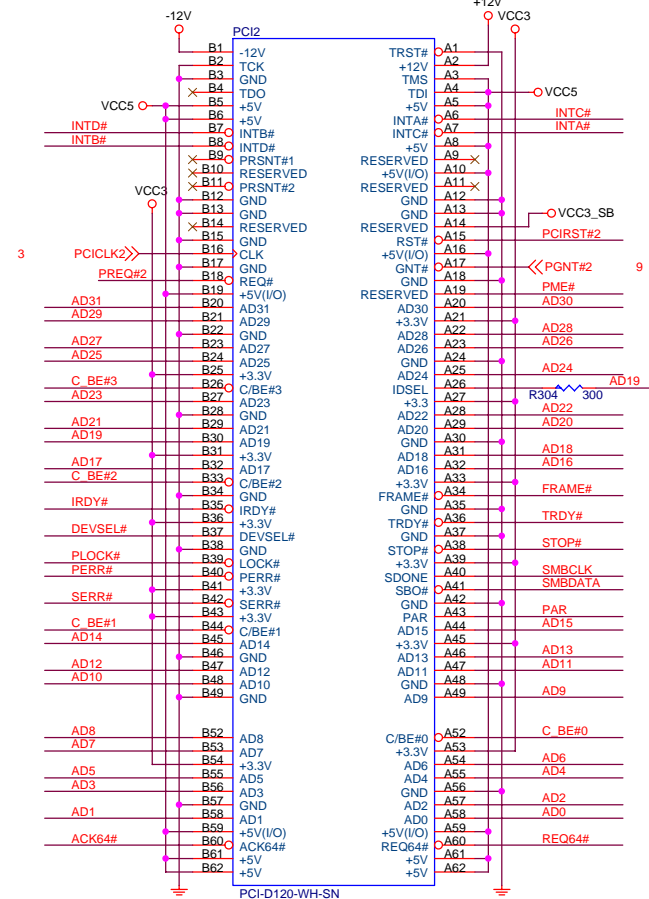
Rev

1B

Date: Friday, January 14, 2005

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PCI SLOT 2 (PCI VER: 2.2 COMPLY)

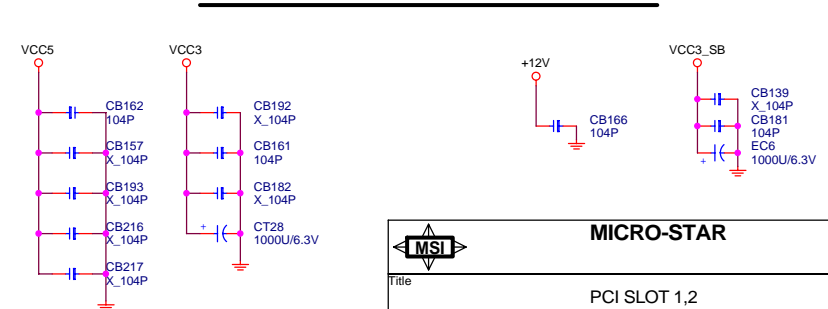


```

IDSEL = AD19
MASTER = PREQ2
INTC#

```

PCI SLOT DECOUPLING CAPACITORS



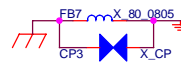
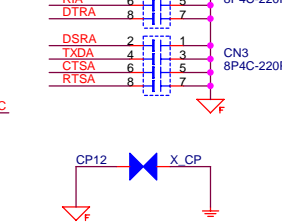
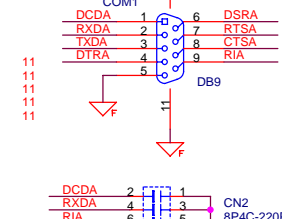
MICRO-STAR

PCI SLOT 1,2

MS-7120

1B

Pinout diagram for the 75232-1 component. The component has two rows of pins. The top row (pins 1-12) includes VCC, RIN1, RIN2, RIN3, RIN4, RIN5, ROUT1, ROUT2, ROUT3, ROUT4, ROUT5, and V-. The bottom row (pins 13-20) includes DIN1, DIN2, DIN3, DIN4, DIN5, DOUT1, DOUT2, DOUT3, DOUT4, DOUT5, and GND. External components shown include a +12VDC supply connected to pin 1 through a 104pF capacitor (CB20), and a -12VDC supply connected to pin 19 through a 0.1uF capacitor (C47). Signal lines are shown for DCDATA#, SINA, RIA#, CTSA#, DSRA#, DTRA, RTSA, and TXDA.



COM2 HEADER

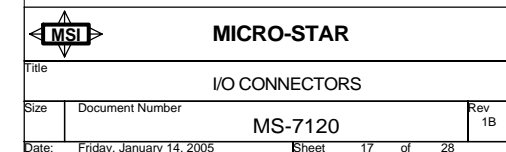
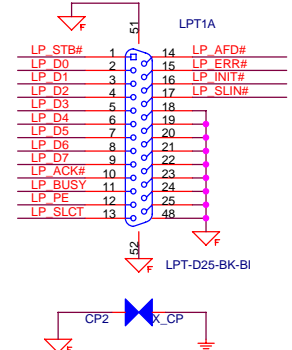
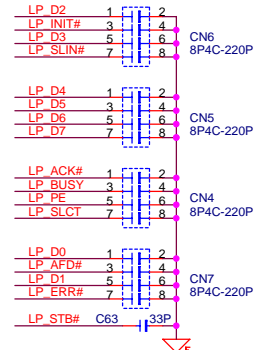
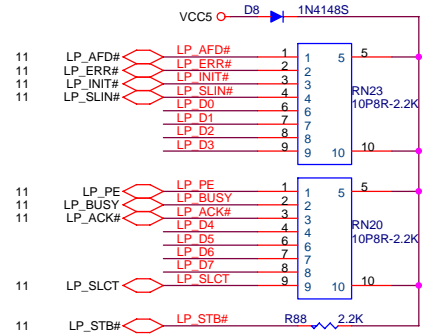
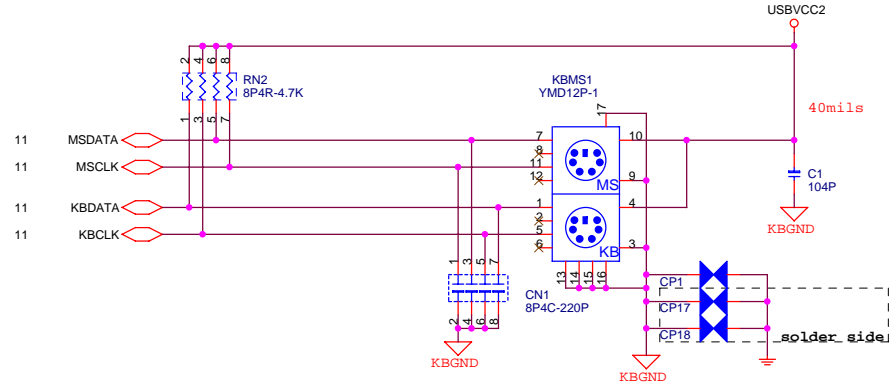
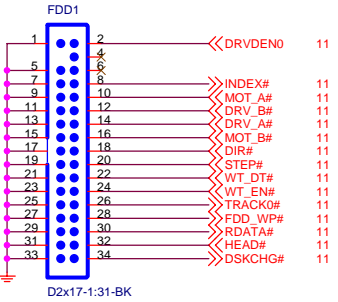
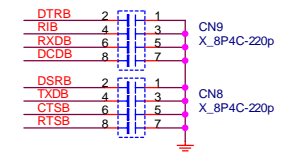
DCDB
TXDB
RTSB
RIB

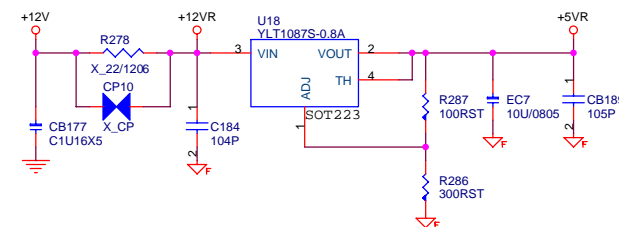
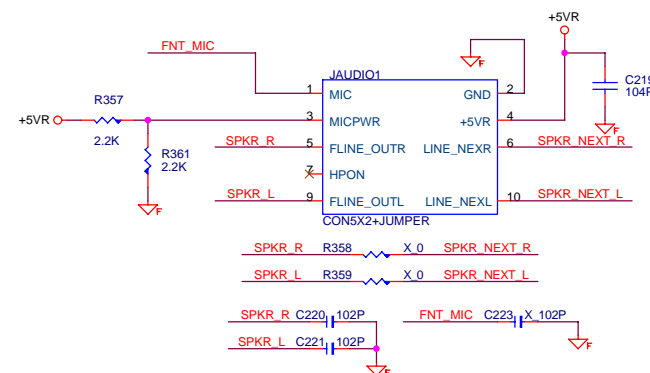
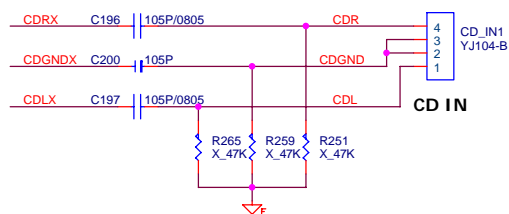
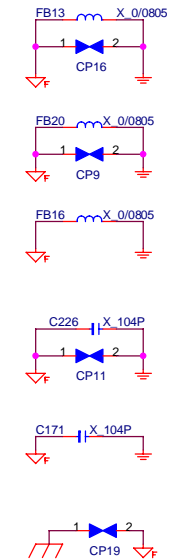
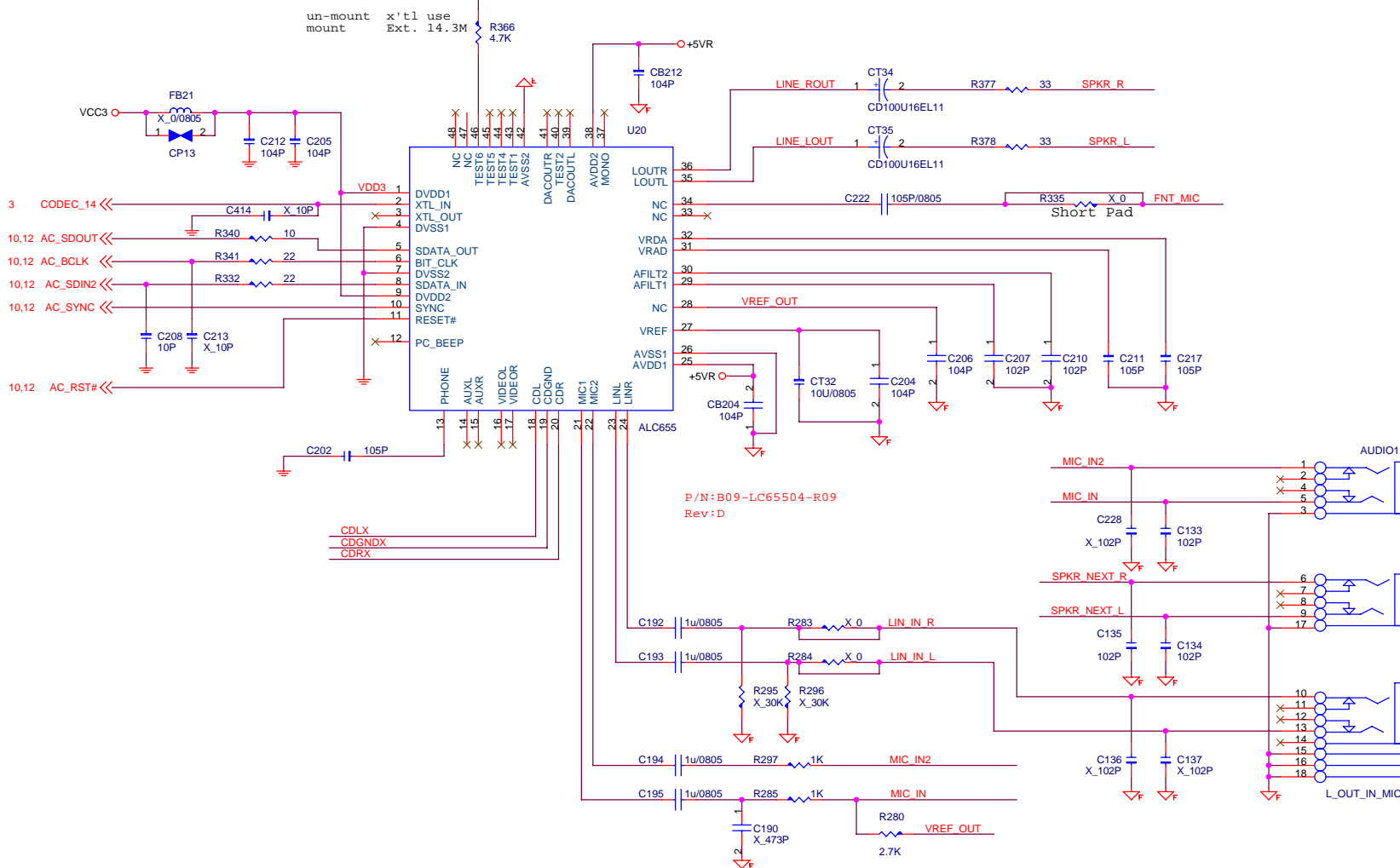
JCOM2

1 2
3 4
5 6
7 8
9

RXDB
DTRB
DSRB
CTB

CON5x2-white

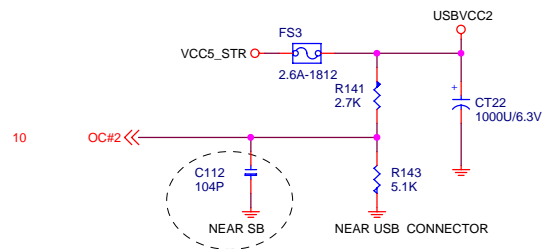




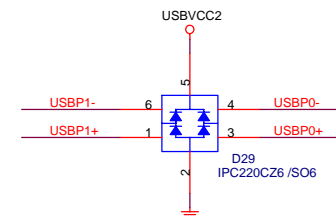
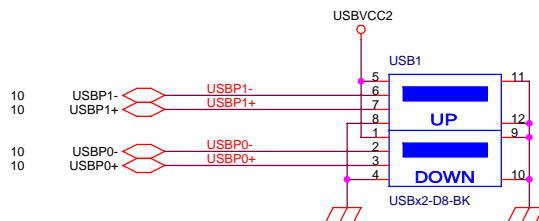
Size	Document Number
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Date: Friday, January 14, 2005 Sheet

POWER CIRCUIT FOR USB PORT 0~3

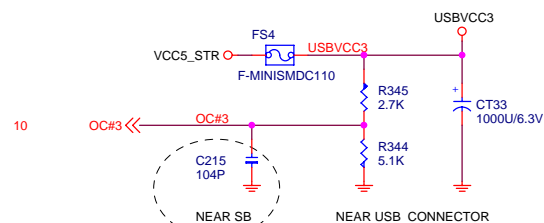


REAR PANEL USB CONNECTOR FOR USB PORT 0,1

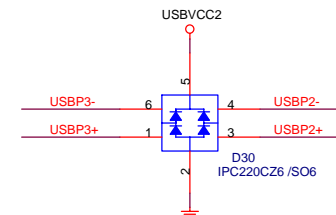
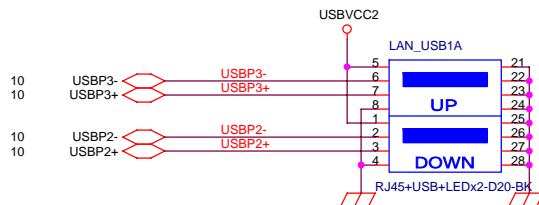


NEAR USB CONNECTOR

POWER CIRCUIT FOR USB PORT 4,5

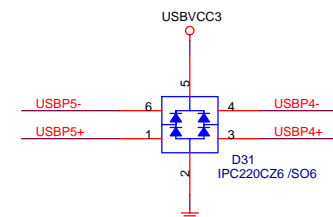
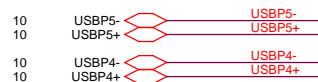


REAR PANEL USB CONNECTOR FOR USB PORT 2,3



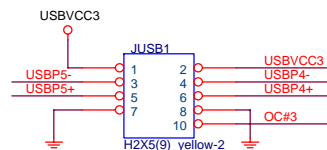
NEAR USB CONNECTOR

FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



NEAR USB CONNECTOR

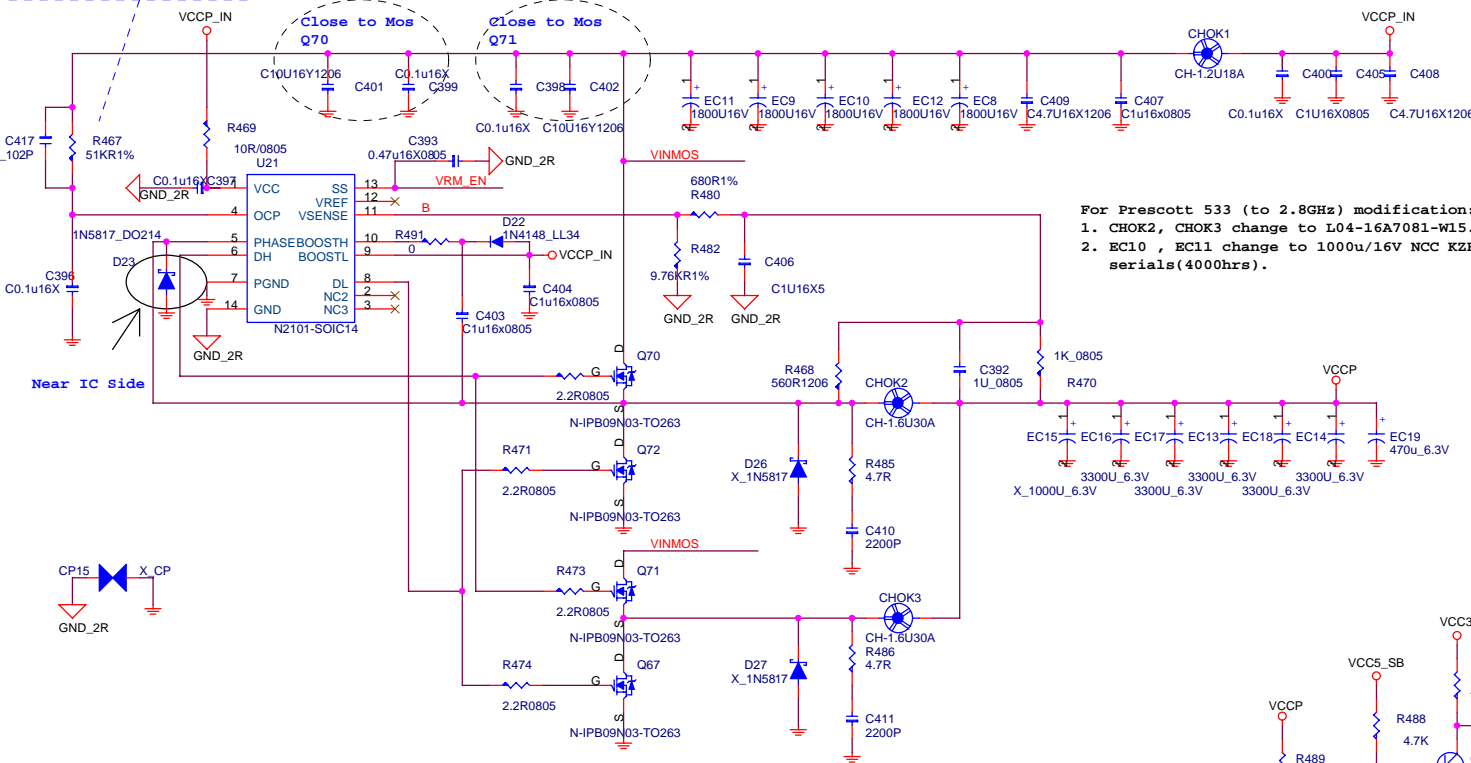
- * USB Trace width : 7.5 mils
- * USB Trace Spacing : 20 mils
- * Differential USB Signal Trace, Spacing : 7.5 mils
- * USB Power Trace must be 50mils width



Intel Front USB Header

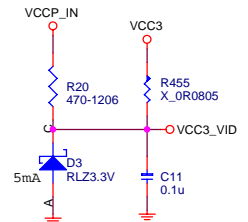
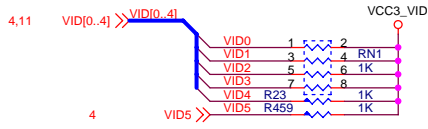
		MICRO-STAR	
Title: USB CONNECTORS			
Size:	Document Number:		Rev: 1B
		MS-7120	
Date:	Friday, January 14, 2005	Sheet	19 of 28

R467 infect the OCP point & switching frequency.

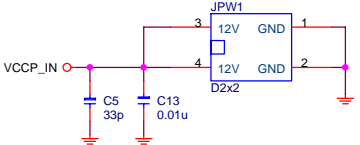


For Prescott 533 (to 2.8GHz) modification:
1. CHOK2, CHOK3 change to L04-16A7081-W15.
2. EC10, EC11 change to 1000u/16V NCC KZE serials(4000hrs).

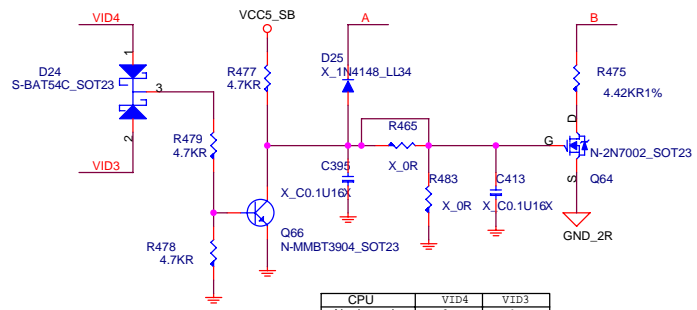
VID PULL-UP RESISTORS



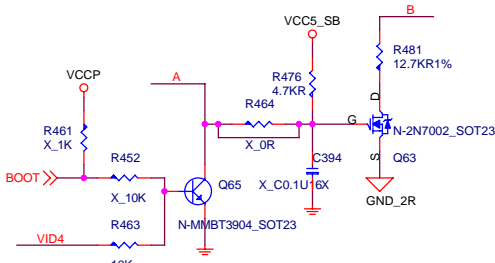
ATX12V POWER CONNECTOR



For Willamette CPU Offset Voltage Adjust

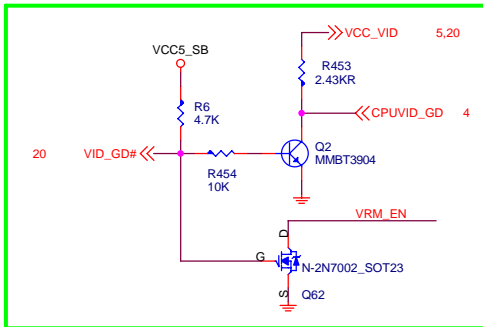


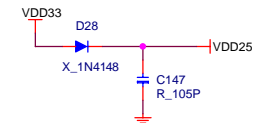
CPU	VID4	VID3
Northwood	0	1
Willamette	0	0
Prescott	1	0



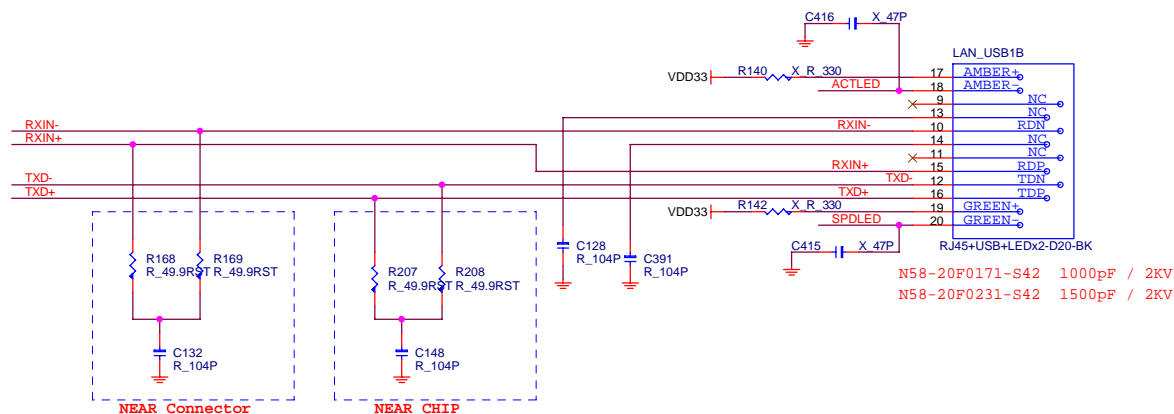
BOOTSEL	CPU
LOW	Northwood
HIGH	Prescott

PWM GOOD

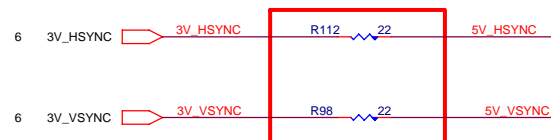
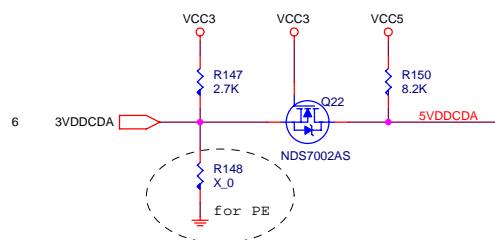
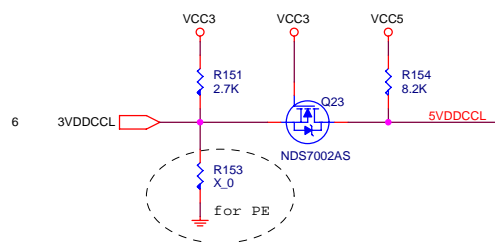
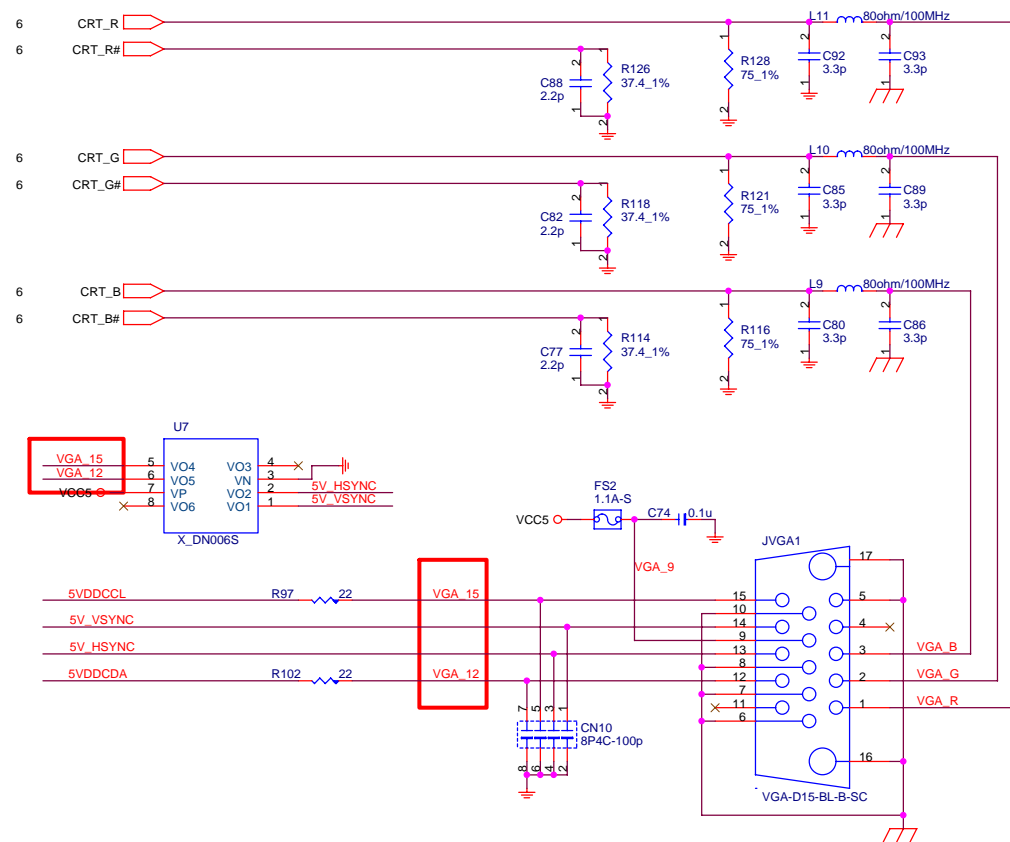





9,15,16

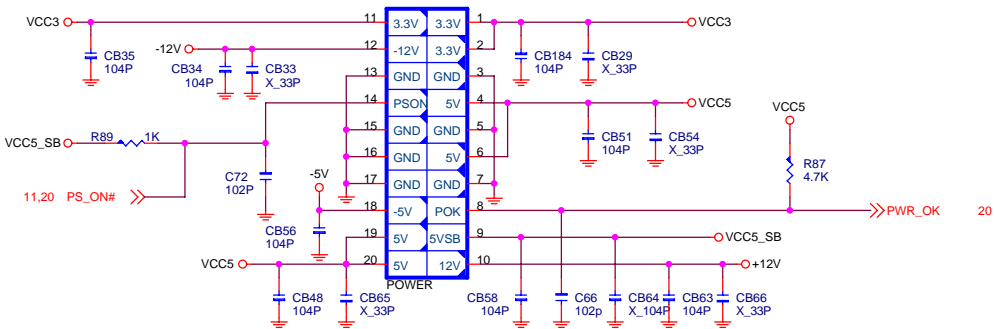


Video Connector

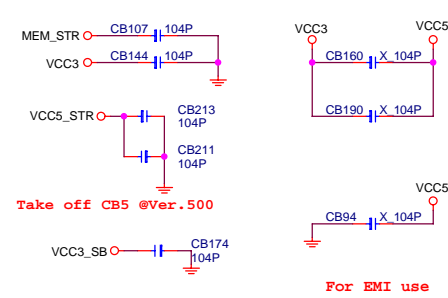


		MICRO-STAR	
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VGA CONNECTOR			
Size	Document Number		Rev
	MS-7120		1B
Date:	Friday, January 14, 2005	Sheet	23 of 28

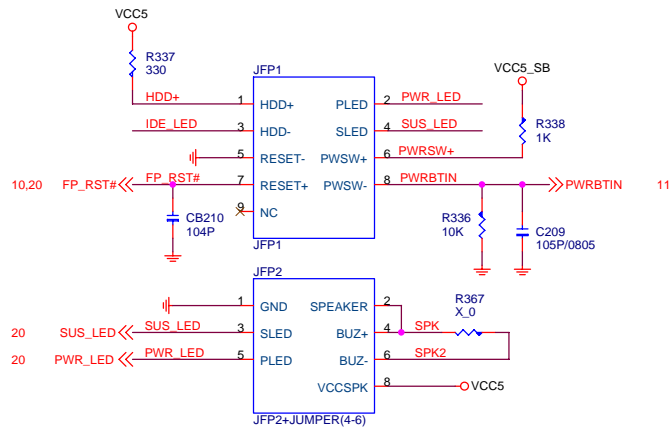
ATX CONNECTOR



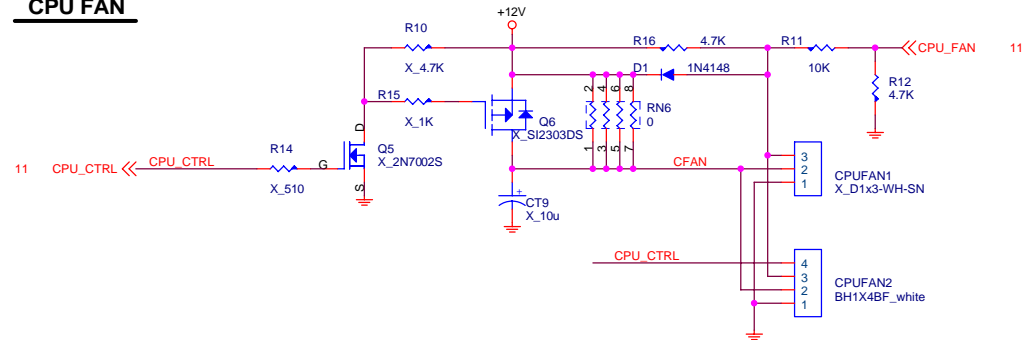
REGULATORS OUTPUT DECOUPLING CAPACITORS



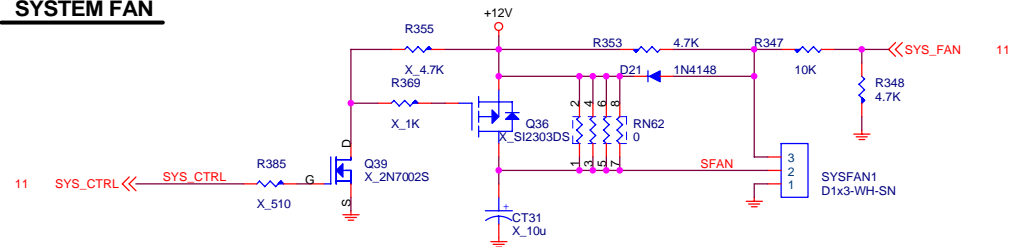
Intel Front Panel



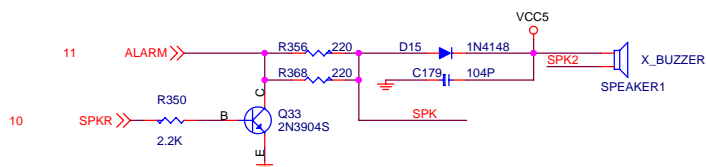
CPU FAN



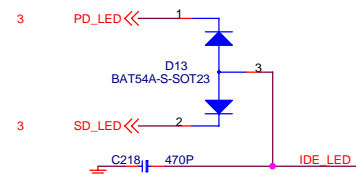
SYSTEM FAN



BUZZER



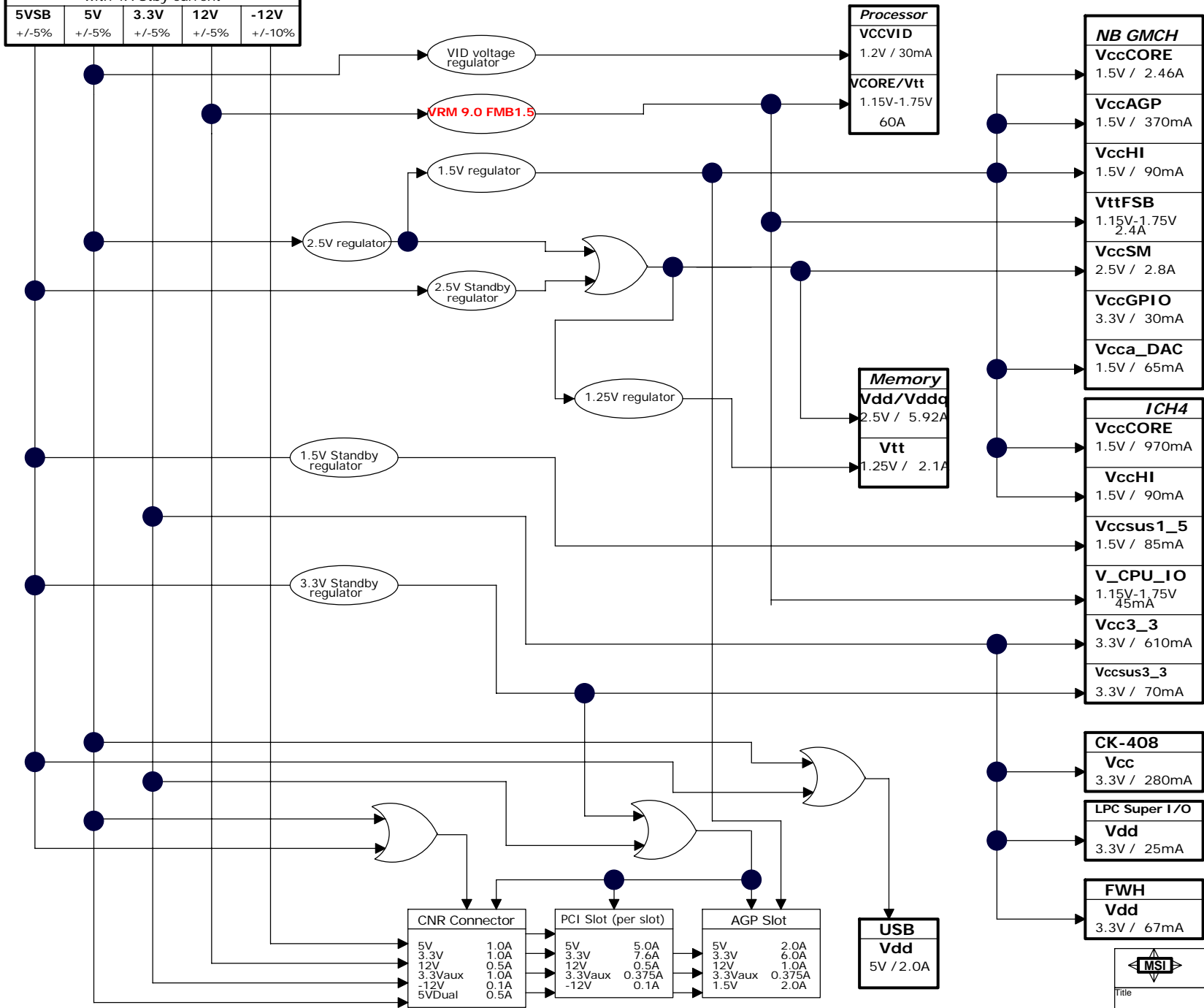
IDE LED



MSI MICRO-STAR			
Title Front Panel & ATX Connector & FAN			
Size	Document Number		Rev
	MS-7120		1B
Date:	Friday, January 14, 2005	Sheet	24 of 28

Power Delivery Map

ATX P/S with 1A Stby current				
5VSB	5V	3.3V	12V	-12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-10%



MICRO-STAR

Title Power Delivery Map		
Size	Document Number MS-7120	Rev 1B
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GPIO SPEC

ICH4

GPIO Pin	Type	Function
GPIO 0	I	REQ#A (multifunction pin)
GPIO 1	I	REQ#B (multifunction pin)
GPIO 2	I	Pull up through 8.2K ohms (PIRQE#)
GPIO 3	I	Pull up through 8.2K ohms (PIRQF#)
GPIO 4	I	Pull up through 8.2K ohms (PIRQG#)
GPIO 5	I	Pull up through 8.2K ohms (PIRQH#)
GPIO 6	I	Pull down through 10K ohms (unused)
GPIO 7	I	Pull down through 10K ohms (unused)
GPIO 8	I	Pull Up to 3.3VSBY through 4.7K ohms (SIO_PME)
GPIO 9	I	Not Implemented
GPIO 10	I	Not Implemented
GPIO 11	I	SMB_ALERT (multifunction pin)
GPIO 12	I	EXTSMI# with Pull up 10K ohms to VCC3_SB
GPIO 13	I	Pull down through 10K ohms (unused)
GPIO 14~15	I	Not Implemented
GPIO 16	O	GNT#A (multifunction pin)
GPIO 17	O	GNT#B (multifunction pin)
GPIO 18	O	No Connected
GPIO 19	O	No Connected
GPIO 20	O	No Connected
GPIO 21	O	No Connected
GPIO 22	OD	No Connected
GPIO 23	O	Pull Up to 3.3V through 8.2K ohms (BIOS protect)
GPIO 24	I/O	GPIO 24
GPIO 25	I/O	GPIO 25
GPIO 26	I/O	Not Implemented
GPIO 27	I/O	No Connected
GPIO 28	I/O	No Connected
GPIO 29~31	O	Not Implemented
GPIO 32	I/O	No Connected
GPIO 33	I/O	No Connected
GPIO 34	I/O	Primary IDE ATA66/100 detection (PD_DET)
GPIO 35	I/O	Secondary IDE ATA66/100 detection (SD_DET)
GPIO 36	I/O	No Connected
GPIO 37	I/O	No Connected
GPIO 38	I/O	No Connected
GPIO 39	I/O	No Connected
GPIO 40	I/O	No Connected
GPIO 41	I/O	No Connected
GPIO 42	I/O	No Connected
GPIO 43	I/O	No Connected
GPIO 44~47	I/O	Not Implemented

FWH

GPIO Pin	Type	Function
GPI 0	I	Pull down through 8.2K ohms (unused)
GPI 1	I	Pull down through 8.2K ohms (unused)
GPI 2	I	P1 customer defined
GPI 3	I	P1 customer defined
GPI 4	I	Pull down through 8.2K ohms (unused)

PCI Config.

DEVICE	ICH INT Pin	IDSEL	CLOCK	CLK GEN PIN OUT
AGP1	INTA# INTB#	AD16	PCICLK0	10 (PCI3/FS4)
PCI Slot 1	INTB# INTC# INTD# INTA#	AD18	PCICLK1	11 (PCI4)
PCI Slot 2	INTC# INTD# INTA# INTB#	AD19	PCICLK2	12 (PCI5)
PCI LAN	INTF# INTG#	AD29	LAN_PCLK	17 (PCI9)

*ICH4 reserved PCI address line AD22 for the PCI-to-ISA Bridge's IDSEL input.

DIMM Config.

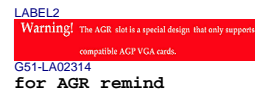
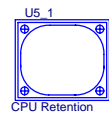
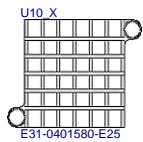
DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	DCLK0/DCLK0# DCLK1/DCLK1# DCLK2/DCLK2#
DIMM 2	1010001B	DCLK3/DCLK3# DCLK4/DCLK4# DCLK5/DCLK5#



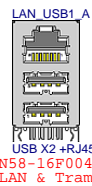
MICRO-STAR

Title GPIO SPEC		
Size	Document Number MS-7120	Rev 1B
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Manual Parts



Option Parts



0A change to 1.0 note :

- 1. Change AGP-slot pin-A11 to floating for AGP8X support. ---- page 15
- 2. Add 0.1u cap for CPU_TMP to GND to avoid noise when SIO detect CPU temperature.(also reserved one for SYS_TMP) ---- page 11
- 3. Audio Line-in damping-resistor change to 0-ohm from 24K-ohm to meet audio-precision THD+N spec. ---- page 18
- 4. Change USB power fuse from 0-ohm resistor to polyswitch. ---- page 19
- 5. Add pci-slot ACK64# & REQ64# pull-up resistor for 64Bit PCI-card compatibility. ---- page 16

100 change to 1.A note :

- 1. Add USB ESD diode D29,D30,D31 for front & rear ports. ---- page 19

1A change to 1B note :

- 1. Change ACPI controller MS5 to MS7-RBC. ---- page 20

MICRO-STAR			
Title			
JUMPER SETTING & MANUAL PARTS			
Size	Document Number		Rev
	MS-7120		1B
Date:	Friday, January 14, 2005		Sheet 28 of 28
			1